UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,712	08/26/2003	Fan Ren	5853-274	6164

30448 7590 09/28/2004

AKERMAN SENTERFITT
P.O. BOX 3188
WEST PALM BEACH, FL 33402-3188

EXAMINER	
BAUMEISTER, BRADLEY W	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,712	REN ET AL.	
	Examiner	Art Unit	
	B. William Baumeister	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/12/03; 1/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2 and 5-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawai '169. Kawai discloses various GaN-based enhancement-mode MOSFETS (i.e., MOSFETs that are in the off-state when the gate is not biased). See e.g., the third embodiment depicted in FIGs 9 and 10, which includes: a GaN comprising layer (GaInN electron transit layer 23b); a IIIGaN (electron supply) layer 23a that is less than 20 nm (e.g., 3 nm) thick (col. 89, lines 1-5); an AlN gate insulating/dielectric film 4 that is preferably 1-10 nm thick (col. 12, lines 1-5, and may be 3 nm thick e.g., col. 4, lines 34-36); and a gate electrode 7 formed thereover.

a. Please note that while the term "MOSFET" is strictly defined as including an oxide insulator, the term is sometimes used more loosely to be synonymous with the broader, generic term "MISFET" that also includes insulators other than oxides. Applicant's inclusion of silicon nitride as a potential species for the gate insulator (see e.g., dependent claim 14) indicates that applicant is employing the broader definition of "MOSFET," including non-oxide gate insulators. As such, the AlN gate insulator of Kawai reads on applicant's definition.

b. Regarding claim 2 and 13, Kawai discloses that the electron supply films 23a, may alternatively be composed of AlGaN (e.g., col. 12, line 26).

c. Regard claims 5, 6, 8 and 13, while the third embodiment depicts an n-channel FET (wherein the carrier supply layer is n-doped to supply electrons), Kawai sates that the device may alternatively be a p-channel FET (e.g., col. 12, lines 57-60).

d. Regarding claim 7, an undoped, 1-nm-thick spacer layer—composed of the same material as the electron supply layer—may be interposed between the electron supply layer and the electron transit layer (e.g., col. 12, lines 44-).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 3 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kawai '169 as applied to the claims above.

a. Kawai discloses that the gate insulating film may be composed of AlN or AlxGa1-xN ($0.3 < x < 1$) (col. 11, lines 38-52). Kawai also discloses that the electron supply layer (1) has a composition/bandgap that is intermediate to those of the AlN-based gate insulating film and the electron transit layer (e.g., Fig 10); and (2) may be composed of AlGaN (e.g., col. 12, line 26), but does not expressly state that in such a case the Al concentration of the electron supply layer may be within 0.2 to 0.35.

b. Nonetheless, setting the Al concentration to be within this particular range is either implicitly disclosed, or at least it would have been obvious to the skilled artisan to have done so, because if the Al concentration was set above 0.3 it would start to become to resistant (col. 1, lines 50); but if it were alternatively set to low, the electron supply layer would not form a sufficiently large heterointerface bandgap with the adjacent channel (or electron transit) layer.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai '169 as applied to the claims above. Regardless of whether Kawai expressly or implicitly discloses that the electron supply layer 23a may further include B, it would have been obvious to one of ordinary skill in the art at the time of the invention to have further included B for either of the well-known purposes of further increasing the supply/channel heterointerface bandgap, adjusting the supply layer's lattice constant, hardness or thermal conductivity.

6. Claims 1-13 are alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai et al. '169 as applied to the claims above, and further in view of Kolodzey et al. '194.

a. In the event that the term "MOSFET" must be interpreted more strictly to be limited to FETs whose gate insulators are composed specifically of oxides, Kawai would not anticipate the claims because the gate insulator thereof is composed of AlN.

b. Kolodzey teaches GaN-based FETs wherein the gate insulator layer is formed by depositing an AlN layer to a thickness of less than 10 nm, and subsequently oxidizing it into aluminum oxide of approximately the same thickness (e.g., col. 3, lines 44-47).

c. It would have been obvious to one of ordinary skill in the art at the time of the invention to have oxidized the AlN gate insulator of Kawai for the purpose of enabling the resultant MOSFET to operate at significantly higher temperatures, as taught by Kolodzey (e.g., col. 3, lines 10-16).

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai '169 as applied to the claims above, and further in view of Hong et al. '357.

a. Kawai discloses all of the limitations except for the gate oxide being composed of one of the materials set forth in claim 14.

b. Hong teaches GaN-based, p-channel or n-channel, enhancement-mode MOSFETs (e.g., col. 4, lines 47-57) having a gate oxide that has a thickness of less than 5nm (e.g., col. 3, line 27; col. 7, line 47), and is composed of Sc2O3 (e.g., col. 6, lines 31, 54 and 60).

c. It would have been obvious to one of ordinary skill in the art at the time of the invention to have substituted Sc2O3 for the AlN gate insulator of Kawai for the purpose of increasing the devices dielectric constant as taught by Hong (e.g., ABSTRACT), or alternatively to allow the device to be operated at higher temperatures as taught by Kolodzey.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to B. William Baumeister whose telephone number is (571) 272-1722. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BRADLEY BAUMEISTER
PRIMARY EXAMINER

B. William Baumeister
Primary Examiner
Art Unit 2815

September 25, 2004